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EXAMINER
PROCTOR, JASON SCOTT

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,142	LEHNER ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,7,8,10,12,13,16,18 and 19* is/are pending in the application.

4a) Of the above claim(s) *21-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,7,8,10,12,13,16,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1, 4-5, 7-8, 10, 12-13, 16, 18-19 were rejected in Office Action of 6 February 2006. Claims 21-27 were subject to a restriction requirement.

In response dated 8 May 2006, Applicants have amended claims 1, 4-5, 7, 10, and 16. Claims 21-27 have been withdrawn. Claims 1, 4-5, 7-8, 10, 12-13, 16, and 18-19 are pending in this application.

Claims 1, 4-5, 7-8, 10, 12-13, 16, and 18-19 are rejected.

Restriction/Election

1. Claims 21-27 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 8 May 2006.

Claim Objections

The previous objections to the claims are withdrawn in response to Applicants' amendments to the claims.

Applicants are respectfully reminded of the requirements found in 37 CFR 1.121(c), which states, "Each amendment document that includes a change to an existing claim, cancellation of an existing claim or addition of a new claim, must include a complete listing of all claims ever presented, including the text of all pending and withdrawn claims, in the

application." (emphasis added) The current listing of the claims is non-compliant with 37 CFR 1.121(c) because the text of withdrawn claims is not presented.

In the interest of compact prosecution, this non-compliance will be disregarded. Future submissions will be required to fully comply with 37 CFR 1.121.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1, 4-5, 7-8, 10, 12-13, 16, and 18-19 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Independent claims 1, 10, and 16 recite a "black box circuit" or "black box circuit model" in several instances. There appears to be no support for a "black box circuit" or "black box circuit model" in the application as originally filed.

Claim 1 recites "a code module which is created by a program compiler, which compiles a plurality of recorded functions to form the code module." There appears to be no support for the claimed program compiler in the application as originally filed. Alternatively, if the claims refer to an ordinary, well known "program compiler," clarification of that fact is requested.

Claim 1 recites the limitation "wherein the user is prevented from supplying inputs, output, and load parameters directly to the simulator module." There appears to be no support for this claimed limitation in the application as originally filed.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 10-12 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The preamble of claim 10 recites "A method of modeling an integrated circuit as a black box circuit so that the integrated circuit details remain hidden **then** simulating the integrated circuit using the black box circuit model comprising the steps of..." which renders the claim vague and indefinite. It appears that the preamble attempts to define method steps. This style of preamble is unconventional and it is unknown how to properly construe the claim.

Alternatively, the preamble describes a process ("modeling an integrated circuit ... then simulating the integrated circuit ... comprising the steps of...") that may be defined by the recited steps. If that is Applicants' position, the Examiner respectfully requests that Applicants consider redrafting the preamble of the claim to avoid confusion.

Claim 13 recites "wherein said step of assigning said parameters to said code module comprises the step of providing a call-back function" which renders the claim vague and indefinite. It appears that claim 13 defines the step of "assigning" from claim 10 as reading:

> assigning inputs, outputs, and load parameters to said code module by calling said code module through said interface and providing a call-back function.

The meaning and result of this limitation are unknown. There appears to be a discrepancy between the actor of claim 10, which "assigns inputs...," and the actor of claim 13, which "provides a call-back function," the former apparently a computer user and the latter presumably a component of computer software. The precise meaning of claim 13 is unknown and clarification is respectfully requested.

4. Claim 19 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 19 recites "wherein said step of assigning said parameters to said code module comprises the step of providing a call-back function" which renders the claim vague and indefinite. It appears that claim 19 defines the step of "assigning" from claim 16 as reading:

> assigning inputs, outputs, and load parameters to said code module by calling said code module through said interface and providing a call-back function.

The meaning and result of this limitation are unknown. There appears to be a discrepancy between the actor of claim 16, which "assigns inputs...," and the actor of claim 19, which "provides a call-back function," the former apparently a computer user and the latter presumably a component of computer software. The precise meaning of claim 19 is unknown and clarification is respectfully requested.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

Claim Rejections - 35 USC § 101

35 U.S.C. § 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1, 4-5, 7-8, 10, and 12-13 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1, 4-5, and 7-8 are directed to "a computerized simulation system" comprising "a simulator module," "a code module," and "an interface." There is no requirement for any tangible hardware components in the claim. In light of the specification, which is primarily directed to computer software, claims 1, 4-5, and 7-8 define a computer *software* "system" and are therefore nonstatutory as reciting functional descriptive material *per se*. Please see MPEP 2106.

Claims 10 and 12-13 define a method that fails to produce a useful, concrete, and tangible result as established in MPEP 2106(II)(A). Although the recited steps fail to achieve either "simulating" or "modeling," these acts also fail to produce a useful, concrete, and tangible result in isolation. In light of the specification, which is primarily directed to computer software, the recited steps of "adding an interface to said code module," and "assigning inputs, outputs, and load parameters," etc., define steps of a nonstatutory software method. In order for such a

method to meet the requirements of 35 U.S.C. § 101, the method must be limited to a practical application and it must produce a useful, concrete, and tangible result.

In response, Applicants' argue primarily that (emphasis in original):

> Applicant has amended [claims] 1, 4-5, and 7-8 to specifically claim statutory subject matter in the form of a computerized simulation system that includes a *tangible* computer system (see Lehner Fig. 8), a *tangible* integrated circuit design to be simulated (inherent in the invention), and a *tangible* black box circuit model (see Lehner Figures 3-5) used to perform the useful art of circuit simulation. The black box circuit model is tangible because it can be built in hardware using basic electrical components including resistors, capacitors, diodes, transistors and other basic circuit elements. The "simulator module", "code module", and "interface" are tangibly embodied in the computer system as machine readable code. Applicants submit that machine readable code is inherent in all computer systems.

The Examiner respectfully traverses this argument as follows.

Contrary to Applicants' arguments, claim 1 recites "A computerized simulation system" and makes no reference, explicit or implicit, to a "tangible computer system." The Examiner maintains the interpretation that claims 1, 4-5, and 7-8 define a computer *software* system and are therefore nonstatutory. Claims 1, 4-5, and 7-8 therefore define computer software and are nonstatutory.

Although an integrated circuit is tangible, an integrated circuit *design* is intangible. For example, the abstract, mental circuit design of two resistors connected in parallel is a circuit *design*, but it is not a tangible circuit.

The Examiner agrees that a "black box model" can be built in hardware, however this observation is not germane to the issue at hand. As with an integrated circuit design, a "black box model" of an integrated circuit is intangible. For example, the abstract, mental "black box model" of a circuit that implements a voltage divider is a "black box model," but it is not a tangible object.

Applicants' arguments [*"The 'simulator module', 'code module', and 'interface' are tangibly embodied in the computer system as machine readable code."*] demonstrate that the invention of claims 10 and 12-13 is computer software *per se*. Claims 10 and 12-13 require no tangible computer hardware. Claims 10 and 12-13 are nonstatutory.

To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. § 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 5, 7, 10, 12-13, 16, and 18-19 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,077,304 to Kasuya.

Regarding claim 1, Kasuya discloses:

A simulator module comprising an API [*"The HDL circuit simulator 102 includes an application program interface (API) 110 that enables other programs to control the operation of the HDL circuit simulator 102 through the use of pre-established instructions (actually procedure calls)."* (column 4, lines 7-11)];

wherein said API comprises at least one function [*"procedure calls"* (column 4, lines 7-11)] and wherein said simulator module uses said function to define a component of the black box circuit and its corresponding simulated behavior [*"The HDL circuit simulator 102 includes a simulation engine 112 that simulates the operation of the circuit specified by the HDL circuit specification 106 received from the system's user via a user interface procedure 114 that handles communications with a user via a computer user interface 115 (hereinafter collectively called the user interface 114, 115)."* (column 4, lines 25-32)];

And wherein said function is recorded as a recorded function and said recorded function, when called during a simulation, reproduces a behavior corresponding to the black box circuit [*supra* (column 4, lines 25-32)];

A code module which is created by a program compiler, which compiles a plurality of recorded functions to form the code module, wherein the code module makes calls to the simulator module during simulation of the black box circuit [*"Each test bench is initially prepared as a test bench source file 130, which is then processed by a test bench compiler 132 so as to generate an executable test bench object file."* (column 5, lines 3-6); *"The test bench object file is executed in conjunction with a verification engine 136 that control and coordinates the tasks performed by the circuit verification subsystem 104. A test bench is a computer program, and thus can perform any operation, sequence of operations, and/or combination* [of] *operations, that the circuit verification subsystem 104 is capable of performing."* (column 5, lines 7-13)]; and

An interface between said code module and a user program wherein a user defines said code module inputs, outputs, and load parameters, and wherein the user is prevented from

supplying inputs, output, and load parameters directly to the simulator module [*"The performance of the specified circuit as simulated by the simulation engine 112 is also determined by the waveforms of the specified circuit's input signals. The input signal waveforms can be specified by the user via the user interface 114, 115, or can be specified through the API 110 through the use of predefined procedure calls for defining input signal waveforms."* (column 4, lines 38-45)].

Regarding claim 5, Kasuya discloses that the interface between the user program and code module includes a dynamic callback function which defines the load parameters [*"The HDL circuit simulator 102 includes a simulation engine 112 that simulates the operation of the circuit specified by the HDL circuit specification 106 received from the system's user via a user interface procedure 114 that handles communications with a user via a computer user interface 115 (hereinafter collectively called the user interface 114, 115)."* (coliumn 4, lines 26-32)].

Regarding claim 7, Kasuya discloses that the code module is compiled into a library [*"Each test bench is initially prepared as a test bench source file 130, which is then processed by a test bench compiler 132 so as to generate an executable test bench object file 134."* (column 5, lines 3-6)].

Claim 10 recites the method performed by the system of claim 1. As Kasuya anticipates the system of claim 1, Kasuya similarly anticipates the method performed by that system.

Claim 12 recites the method corresponding to the system of claim 7. As Kasuya anticipates the system of claim 7, Kasuya similarly anticipates the method performed by that system.

Regarding claim 13, the precise meaning of the recited limitations is unknown. However, Kasuya discloses a function for communication between the user interface and the code module [*"The HDL circuit simulator 102 includes a simulation engine 112 that simulates the operation of the circuit specified by the HDL circuit specification 106 received from the system's user via a user interface procedure 114 that handles communications with a user via a computer user interface 115 (hereinafter collectively called the user interface 114, 115)."* (coliumn 4, lines 26-32)].

Claim 16 recites a program storage device storing instructions that perform the method of claim 1. As Kasuya anticipates the system of claim 1 and further discloses a computer system [*"In the preferred embodiment, the HDL circuit simulator 102 and the circuit operation verifier 104 are executed by the same CPU 108, and in fact operate together in most respects as a single program. Suitable operating systems 109 include, for example, UNIX [...], Solaris [...], and Windows NT [...]."* (column 3, line 66 – column 4, line 6)], Kasuya similarly anticipates the program storage device storing instructions that perform the method of claim 1.

Claim 18 recites the method corresponding to the system of claim 7. As Kasuya anticipates the system of claim 7, Kasuya similarly anticipates the program storage device storing instructions that perform the method of claim 7.

Regarding claim 19, the precise meaning of the recited limitations is unknown. However, Kasuya discloses a function for communication between the user interface and the code module [*"The HDL circuit simulator 102 includes a simulation engine 112 that simulates the operation of the circuit specified by the HDL circuit specification 106 received from the system's user via a user interface procedure 114 that handles communications with a user via a computer user interface 115 (hereinafter collectively called the user interface 114, 115)."* (coliumn 4, lines 26-32)].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was

commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

7. Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kasuya in view of "IEEE 100 The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition" (IEEE 100).

Regarding claim 4, Kasuya discloses the invention of claim 1.

Kasuya does not expressly disclose a "static load model".

IEEE 100 discloses a "resistor," described as "An element within a circuit that has a specified resistance value designed to restrict the flow of current," i.e. a *static load.*

Kasuya and IEEE 100 are analogous art because both are directed to electrical engineering.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a *static load* model, for example, a *resistor*, in the circuit simulation system of Kasuya.

The motivation for doing so would have been found in the knowledge of a person of ordinary skill in the art in recognition of the fact that a resistor is a basic and fundamental electrical component that is necessary for the design of almost every useful electrical device.

Therefore, it would have been obvious to combine IEEE 100 with Kasuya to obtain the invention as specified in claim 4.

8. Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kasuya in view of "Microsoft Computer Dictionary, Fifth Edition" (Microsoft Computer Dictionary).

Regarding claim 8, Kasuya discloses the invention of claim 7.

Kasuya does not expressly disclose that the code module comprises a "dynamically loadable library".

Microsoft Computer Dictionary discloses a "dynamic-link library," described as "A feature of the Microsoft Windows family of operating systems and OS/2 that allows executable routines to be stored separately as files with DLL extensions and to be loaded only when needed by a program," i.e. a *dynamically loadable library*.

Kasuya and Microsoft Computer Dictionary are analogous art because both are directed to computer software.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a *dynamically loadable library*, for example, a *dynamic-link library*, in the circuit simulation system of Kasuya.

The motivation for doing so would have been found in the knowledge of a person of ordinary skill in the art in recognition of the fact that a DLL is a standard part of the ubiquitous Microsoft Windows operating system and provides the flexibility innate in storing executable routines in separate files.

Therefore, it would have been obvious to combine Microsoft Computer Dictionary with Kasuya to obtain the invention specified in claim 8.

Response to Arguments

In response to the previous rejections of the claims under 35 U.S.C. § 103, Applicants argue primarily that:

> Applicants submit that Kasuya does not teach a means for ***both "secretly" modeling*** a circuit as a black box ***and precisely simulating*** the original circuit using the black box circuit.

The Examiner respectfully traverses this argument as follows.

None of the pending claims requires "secretly" modeling a circuit. Additionally, the meaning of this phrase as used by Applicants is ambiguous. None of the pending claims requires "precisely" simulating the original circuit. Additionally, the term "precisely simulating" appears to be a relative term that is not defined in the specification, in the claims, or in Applicants' remarks.

Applicants further argue that (emphasis in original):

> The simulation engine described by Kasuya uses ***predefined*** circuit models 116 (i.e. detailed transistor-level models), which are used to represent ***specific circuit components*** and the models are stored in a library (see Kasuya col. 4, lines 25-34). The abstracted models and detailed transistor-level models described by Kasuya, 1. cannot be simulated simultaneously using Kasuya's disclosed method, and 2. cannot provide an accurate simulation result while hiding circuit details.

The Examiner respectfully traverses this argument as follows.

The Examiner fails to see any connection between the citations shown and Applicants' conclusions. Further, the claims are not limited to "non-predefined circuit models" or "generic circuit components."

Applicants further argue that:

> The invention disclosed by Kasuya does not include a circuit module or a simulation module as described by the instant application (see Lehner Fig. 8, amended claims 1, 10, and 16) both of which are key elements of the present invention. Furthermore, none of the other references cited describe a simulation module or a circuit module as described in the instant application. In Kasuya's disclosed invention, the simulator is not hidden from either the simulation verification sub-system 104, or the user via user interface 114 (see Kasuya, Col. 4, lines 26-32).

The Examiner respectfully traverses this argument as follows.

Applicants' arguments amount to a general allegation that the claims define a patentable invention without specifically pointing out how the ***language of the claims*** patentably distinguishes them from the references. The Examiner respectfully requests that Applicants identify which claim limitations require "hiding a simulator".

Applicants further argue that:

> In the instant Application, the circuit module calls the simulator module rather than the simulator module calling the circuit module (see Lehner Fig. 8). Futhermore, the user described in the instant Application does not provide inputs directly to the API simulator. The user supplies inputs only to the code module, which in turn calls the API simulator to reproduce the black box circuit model's behavior (see amended claims 1, 10, and 16 herein).

The Examiner respectfully traverses this argument as follows.

Applicants' arguments directed to the specification are unpersuasive because patentability is based upon what is claimed rather than what is disclosed. There are no pending claims that make any reference to a "circuit module". It is noted that claims 1, 10, and 16 recite "wherein the code module makes calls to the simulator module during simulation." Kasuya anticipates this claim language (column 5, lines 3-45, etc.).

Applicants' arguments have been fully considered but have been found unpersuasive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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